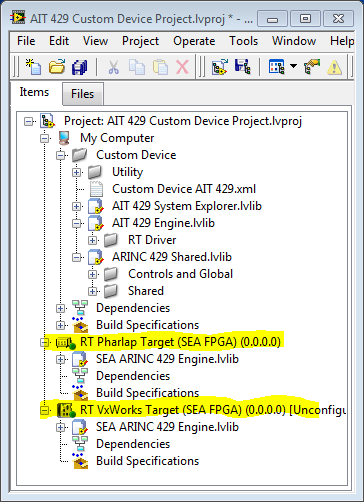
# ARINC 429 CD Changelog

## Dev after 19bca0e

* All development done in LV 2012
* Added Pharlap + VxWorks targets (each including conditional symbol „SEA\_FPGA = TRUE“)
* Mass compiled